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(54) Method of depositing organosilicate layers

(57) A method of forming an organosilicate layer is disclosed. The organosilicate layer is formed by applying an electric field to a gas mixture comprising an organosilane compound and an oxygen-containing gas. The organosilicate layer is compatible with integrated circuit fabrication processes. In one integrated circuit fabrication process, the organosilicate layer is used as an intermetal dielectric layer. In another integrated circuit fabrication process, the organosilicate layer is incorporated into a damascene structure.

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Description

[0001] The present invention relates to organosilicate layers, their use in integrated circuit fabrication, and a method for forming an organosilicate layer.

[0002] Integrated circuits have evolved into complex devices that can include millions of components (e. g., transistors, capacitors and resistors) on a single chip. The evolution of chip designs continually requires faster circuitry and greater circuit density. The demands for greater circuit density necessitate a reduction in the dimensions of the integrated circuit components.

[0003] As the dimensions of the integrated circuit components are reduced (e. g., sub-micron dimensions), the materials used to fabricate such components contribute to their electrical performance. For example, low resistivity metal interconnects (e. g., copper and aluminum) provide conductive paths between the components on integrated circuits. Typically, the metal interconnects are electrically isolated from each other by an insulating material. When the distance between adjacent metal interconnects and/or the thickness of the insulating material has sub-micron dimensions, capacitive coupling potentially occurs between such interconnects. Capacitive coupling between adjacent metal interconnects may cause cross talk and/or resistance-capacitance (RC) delay which degrades the overall performance of the integrated circuit. In order to prevent capacitive coupling between adjacent metal interconnects, low dielectric constant (low k) insulating materials (e. g., dielectric constants less than about 4.5) are needed.

[0004] Therefore, a need exists in the art for low dielectric constant materials suitable for integrated circuit fabrication.

[0005] A method of forming an organosilicate layer for use in integrated circuit fabrication is provided. In one embodiment, the organosilicate layer is formed by applying an electric field to a gas mixture comprising an organosilane compound and an oxygen-containing gas.

[0006] The organosilicate layer is compatible with integrated circuit fabrication processes. In one integrated circuit fabrication process, the organosilicate layer is used as an intermetal dielectric layer. For such an embodiment, a preferred process sequence includes depositing the organosilicate layer over conductive features formed on a substrate.

[0007] In another integrated circuit fabrication process, the organosilicate layer is incorporated into a damascene structure. For such an embodiment, a preferred process sequence includes depositing a first dielectric layer on a substrate. An organosilicate layer is then formed on the first dielectric layer. Thereafter, the organosilicate layer is patterned and etched to define contacts/vias therethrough. After the organosilicate layer is patterned and etched, a second dielectric layer is deposited thereover. The second dielectric layer is then patterned and etched to define interconnects therethrough. The interconnects formed in the second dielectric layer are positioned over the contacts/vias formed in the organosilicate layer. After the interconnects are formed, the contacts/vias defined in the organosilicate layer are etched through the first dielectric layer to the substrate surface. Thereafter, the damascene structure is completed by filling the interconnects and contacts/vias with a conductive material.

[0008] The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a schematic illustration of an apparatus that can be used for the practice of embodiments described herein;

FIG. 2 depicts a schematic cross-sectional view of a chemical vapor deposition (CVD) chamber;

FIGS. 3a-3b depict schematic cross-sectional views of a substrate at different stages of integrated circuit fabrication incorporating an organosilicate layer as an intermetal dielectric layer; and

FIGS. 4a-4e depict schematic cross-sectional views of a damascene structure at different stages of integrated circuit fabrication incorporating an organosilicate layer in such structure.

[0009] FIG. 1 is a schematic representation of a wafer processing system 35 that can be used to perform integrated circuit fabrication in accordance with embodiments described herein. This apparatus typically comprises process chambers 36, 38, 40, 41, load-lock chambers 46, a transfer chamber 50, a microprocessor controller 54, along with other hardware components such as power supplies (not shown) and vacuum pumps (not shown). An example of such a wafer processing system 35 is a CENTURA® System, commercially available from Applied Materials, Inc., Santa Clara, California. Details of the wafer processing system are described in US-A-5,186,718. The salient features of this system 35 are briefly described below.

[0010] The wafer processing system 35 includes a transfer chamber 50, containing a transfer robot 51. The transfer chamber 50 is coupled to load-lock chambers 46 as well as a cluster of process chambers 36, 38, 40, 41. Substrates (not shown) are loaded into the wafer processing system 35 through load-lock chambers 46. Thereafter, transfer robot 51 moves the substrates between one or more of the process chambers 36, 38, 40, 41.

[0011] The process chambers 36, 38, 40, 41 are used to perform various integrated circuit fabrication sequences. For example, process chambers 36, 38, 40, 41 may include physical vapor deposition (PVD) chambers, ionized metal plasma physical vapor deposition (IMP PVD) chambers, chemical vapor deposition (CVD) chambers, rapid thermal process (RTP) chambers, and anti-reflective coating (ARC) chambers, among others.

[0012] FIG. 2 depicts a schematic cross-sectional view of a chemical vapor deposition (CVD) process chamber 36 of wafer processing system 35. CVD process chamber 36 may be used to deposit organosilicate layers in accordance with embodiments described herein. An example of such a CVD process chamber 36 is a DXZ™ chamber, commercially available from Applied Materials, Inc., Santa Clara, California.

[0013] CVD process chamber 36 typically comprises a gas panel 130, a control unit 110, along with other hardware components such as power supplies and vacuum pumps. Details of a CVD process chamber 36 are described in the US patent application Serial No. 09/211,998. The salient features of the CVD process chamber 36 are briefly described below.

[0014] The CVD process chamber 36 generally houses a support pedestal 150, which is used to support a substrate such as a semiconductor wafer 190. This pedestal 150 can typically be moved in a vertical direction inside the chamber 36 using a displacement mechanism (not shown). Depending on the specific process, the wafer 190 can be heated to some desired temperature prior to layer deposition. For example, the wafer support pedestal 150 is heated by an embedded heater element 170. The pedestal 150 may be resistively heated by applying an electric current from an AC supply 106 to the heater element 170. The wafer 190 is, in turn, heated by the pedestal 150. A temperature sensor 172, such as a thermocouple, is also embedded in the wafer support pedestal 150 to monitor the temperature of the pedestal 150 in a conventional manner. The measured temperature is used in a feedback loop to control the power supplied to the heating element 170, such that the wafer temperature can be maintained or controlled at a desired temperature which is suitable for the particular process application. The pedestal 150 is optionally heated using a plasma or by radiant heat (not shown).

[0015] A vacuum pump 102, is used to evacuate the process chamber 36 and to maintain the proper gas flows and pressure inside the chamber 36. A showerhead 120, through which process gases are introduced into the chamber 36, is located above the wafer support pedestal 150. The showerhead 120 is connected to a gas panel 130, which controls and supplies various gases used in different steps of the process sequence.

[0016] The showerhead 120 and wafer support pedestal 150 also form a pair of spaced apart electrodes. When an electric field is generated between these electrodes, the process gases introduced into the chamber 36 are ignited into a plasma. Typically, the electric field is generated by connecting the wafer support pedestal 150 to a source of RF power (not shown) through a matching network (not shown). Alternatively, the RF power source and matching network may be coupled to the showerhead 120, or coupled to both the showerhead 120 and the wafer support pedestal 150.

[0017] Plasma enhanced chemical vapor deposition (PECVD) techniques promote excitation and/or dissociation of the reactant gases by the application of the electric field to the reaction zone near the substrate surface, creating a plasma of reactive species. The reactivity of the species in the plasma reduces the energy required for a chemical reaction to take place, in effect lowering the required temperature for such PECVD processes.

[0018] In at least one embodiment, organosilicate layer deposition is accomplished by plasma enhanced oxidation of a organosilane compound, such as for example, trimethylsilane. The organosilane compound is introduced into the process chamber 36 under the control of gas panel 130 as a gas with a regulated flow.

[0019] Proper control and regulation of the gas flows through the gas panel 130 is performed by mass flow controllers (not shown) and a computer (not shown). The showerhead 120 allows process gases from the gas panel 130 to be uniformly introduced and distributed in the process chamber 100.

[0020] Referring to FIG. 1, the CVD process chamber 36 is controlled by a microprocessor controller 54. The microprocessor controller 54 may be one of any form of general purpose computer processor (CPU) that can be used in an industrial setting for controlling various chambers and sub-processors. The computer may include any suitable memory, such as random access memory, read only memory, floppy disk drive, hard disk, or any other form of digital storage, local or remote. Various support circuits may be coupled to the CPU for supporting the processor in a conventional manner. Software routines as required may be stored in the memory or executed by a second CPU that is remotely located.

[0021] The software routines are executed after the substrate is positioned on the pedestal. The software routine, when executed, transforms the general purpose computer into a specific process computer that controls the chamber operation so that a chamber process is performed. Alternatively, a process of the present invention may be performed in hardware, as an application specific integrated circuit or other type of hardware implementation, or a combination of software or hardware.

Organosilicate Layer Deposition

[0022] In one embodiment, the organosilicate layer is formed by applying an electric field to a gas mixture comprising an organosilane compound and an oxygen-containing gas. The organosilane compound has the general formula $Si_aC_bH_cO_d$ where a has a range between 1 and 2, b has a range between 1 and 10, c has a range between 6 and 30, and d has a range between 0 and 6.

[0023] For example, methylsilane ($SiCH_6$), dimethylsilane (SiC_2H_8), trimethylsilane (SiC_3H_{10}), tetramethylsilane (SiC_4H_{12}), methoxysilane ($SiCH_6O$), dimethyldimethoxysilane ($SiC_4H_{12}O_2$), diethyldiethoxysilane ($SiC_8H_{20}O_2$), dimethyldiethoxysilane ($SiC_6H_{16}O_2$), diethyldimethoxysilane ($SiC_6H_{16}O_2$), hexamethyldisi-

loxane ($Si_2C_6H_{18}O$), bis(methylsilano)methane ($Si_2C_3H_{12}$), 1,2-bis(methylsilano)ethane ($Si_2C_4H_{14}$), among others may be used as the organosilane compound.

[0024] Oxygen (O_2), ozone (O_3), nitrous oxide (N_2O), carbon monoxide (CO), carbon dioxide (CO_2), or combinations thereof, among others, may be used as the oxygen-containing gas. The oxidizing gas may be diluted with an inert gas such as helium (He) and/or argon (Ar).

[0025] In general, the following deposition process parameters can be used to form the organosilicate layer using a CVD process chamber similar to that shown in FIG. 2. The process parameters may include a wafer temperature of about 50 °C to about 500 °C, a chamber pressure of about 1 torr to about 500 torr, an organosilane compound gas flow rate of about 50 sccm to about 1000 sccm, an oxygen-containing gas flow rate of about 10 sccm to about 1000 sccm, and an RF power of between about 1 watts/cm^2 to about 500 watts/cm^2. The above process parameters provide a deposition rate for the organosilicate layer in the range of about 0.1 micron/min to about 2 micron/min when implemented on a 200 mm (millimeter) substrate in a deposition chamber available from Applied Materials, Inc.

[0026] Other deposition chambers are within the scope of the invention, and the parameters listed above may vary according to the particular deposition chamber used to form the organosilicate layer. For example, other deposition chambers may have a larger (e. g., configured to accommodate 300 mm substrates) or smaller volume, requiring gas flow rates that are larger or smaller than those recited for deposition chambers available from Applied Materials, Inc.

[0027] After the organosilicate layer is formed, it is optionally annealed. Nitrogen (N_2), hydrogen (H_2), oxygen (O_2), or combinations thereof, among others, may be used as the annealing gas. It is believed that the annealing step minimizes the water vapor absorption capability of the as deposited organosilicate layer, improving the dielectric properties thereof.

[0028] In general, the following process parameters may be used to anneal the organosilicate layer in a process chamber similar to that shown in Fig. 2. The process parameters range from a wafer temperature of about 200 °C to about 500 °C and an annealing gas flow rate of about 1000 sccm to about 10,000 sccm. The organosilicate layer is annealed for less than about 30 minutes.

[0029] The as-deposited organosilicate layer has a dielectric constant that is less than about 3.0, making it suitable for use as an insulating material in integrated circuits. The dielectric constant of the organosilicate layer is tunable, in that it can be varied in a range between about 2.0 to about 3.0 as a function of the reaction temperature. In particular, as the reaction temperature increases, the dielectric constant of the as-deposited layer decreases.

[0030] The dielectric constant of the organosilicate layer can also be tuned as a function of the composition of the gas mixture during layer formation. As the carbon (C) concentration in the gas mixture increases, the C content of the as-deposited organosilicate layer increases, decreasing its dielectric constant.

Integrated Circuit Fabrication Processes

A. Organosilicate Intermetal Dielectric Layer

[0031] FIGs. 3a-3b illustrate schematic cross-sectional views of a substrate 200 at different stages of an integrated circuit fabrication sequence incorporating an organosilicate layer as an intermetal dielectric layer. In general, the substrate 200 refers to any workpiece on which film processing is performed. Depending on the specific stage of processing, the substrate 200 may correspond to a silicon wafer, or other material layers, which have been formed on the substrate. FIG. 3a, for example, illustrates a cross-sectional view of a substrate structure 250 in which the substrate 200 is a silicon wafer with conductive features 204 formed thereon. The conductive features may be formed of a metal (e. g., copper, aluminum, tungsten).

[0032] The conductive features 204 have various cross-sectional geometries such as, for example, square, rectangular, and circular. The conductive features typically have aspect ratios of greater than about 1:4. The aspect ratio is defined as the feature height divided by its width.

[0033] FIG. 3b depicts an organosilicate layer 206 formed on the substrate structure 250 according to the process parameters described above. The thickness of the organosilicate layer 206 is variable depending upon the specific stage of processing. Typically the organosilicate layer 206 is deposited to a thickness of about 500 Å to about 10000 Å.

[0034] After the organosilicate layer 206 is formed on the substrate structure 250, the organosilicate layer is optionally annealed. The organosilicate layer 206 is annealed according to the process parameters described above.

C. Damascene Structure Incorporating an Organosilicate layer

[0035] FIGS. 4a-4e illustrate schematic cross-sectional views of a substrate 300 at different stages of a damascene structure fabrication sequence incorporating an organosilicate layer therein. Damascene structures are typically used to form metal interconnects on integrated circuits. Depending on the specific stage of processing, substrate 300 may correspond to a silicon substrate, or other material layer that has been formed on the substrate 300. FIG. 4a, for example, illustrates a cross-sectional view of a substrate 300 having conductive features 301, intermetal dielectric 303, a barrier layer 305, as well as a first dielectric layer 302 formed ther-

eon. The conductive features 301 may be a metal (e. g., aluminum, copper). The intermetal dielectric 303 and the barrier layer 305 may be a low dielectric constant material (e. g., organosilicate material, silicon carbide). The first dielectric layer 302 may be an oxide (e. g., silicon oxide, fluorosilicate glass). In general, the substrate 300 may include a layer of silicon, silicides, metals, or other materials.

[0036] FIG. 4a illustrates one embodiment in which the substrate 300 is silicon, the conductive features 301 are copper, and the intermetal dielectric 303 is a silicon oxide. The barrier layer 305 is typically a silicon carbide layer suitable to minimize the diffusion of metal from the conductive features into the first dielectric layer 302. The barrier layer 305 has a thickness of about 200 Å to about 1000 Å, depending on its dielectric constant as well as its etch selectivity with respect to the overlying dielectric material (e. g., the barrier layer preferably has an etch selectivity with respect to the overlying dielectric layer that is greater than about 10:1). The first dielectric layer 302 has a thickness of about 1,000 Å to about 10,000 Å, depending on the size of the structure to be fabricated.

[0037] An organosilicate layer 304 is formed on the first dielectric layer 302. The organosilicate layer 304 is formed on the first dielectric layer 302 according to the process parameters described above. The organosilicate layer 304 has a dielectric constant less than 3.0, so as to prevent or minimize capacitive coupling between the metal interconnects to be formed in the damascene structure. The dielectric constant for the organosilicate layer 304 is tunable, in that it can be varied in the desired range as a function of the reaction temperature as well as the composition of the gas mixture during layer formation.

[0038] The thickness of the organosilicate layer 304 is variable depending on the specific stage of processing. Typically, the organosilicate layer 304 has a thickness of about 200 Å to about 1000 Å, depending on its dielectric constant as well as its etch selectivity with respect to an overlying dielectric material subsequently formed thereon (e. g., the barrier layer preferably has an etch selectivity with respect to the overlying dielectric layer that is greater than about 10:1).

[0039] Referring to FIG. 4b, the organosilicate layer 304 is patterned and etched to define contact/via openings 306 and to expose the first dielectric layer 302, in areas where the contacts/vias are to be formed. The contact/via openings 306 are positioned over the conductive features 301.

[0040] The organosilicate layer 304 may be patterned using conventional lithography process. For example, in a conventional lithography process, a layer of energy sensitive resist material (not shown) is formed on the organosilicate layer 304. The layer of energy sensitive resist material can be spin coated on the substrate to a thickness within a range of about 4000 Å to about 10,000 Å. Most energy sensitive resist materials are sensitive to ultraviolet (UV) radiation having a wavelength less than about 450 nm (nanometers). Deep ultraviolet (DUV) resist materials are sensitive to UV radiation having wavelengths less than about 245 nm.

[0041] An image of a pattern is introduced into the layer of energy sensitive resist material by exposing such energy sensitive resist material to UV radiation via a mask (not shown). The image of the pattern introduced in the layer of the energy sensitive resist material is developed in an appropriate developer to define the pattern therethrough. Thereafter referring to Fig. 4b, the pattern defined in the energy sensitive resist material is transferred through the organosilicate layer 304.

[0042] The pattern is transferred through the organosilicate layer 304 using the energy sensitive resist material (not shown) as a mask. The pattern is transferred through the organosilicate layer 304 using an appropriate chemical etchant. For example, carbon tetrafluoride (CF_4) fluoroethane (C_2F_6), and fluorobutene (C_4F_8) may be used to chemically etch the organosilicate layer 304.

[0043] After the organosilicate layer 304 is patterned, a second dielectric layer 308 is deposited over the organosilicate layer 304, as shown in Fig. 4c. The second dielectric layer 308 may be an oxide (e. g., silicon dioxide, fluorosilicate glass). The second dielectric layer 308 has a thickness of about 1,000 Å to about 10,000 Å, depending on the size of the structure to be fabricated.

[0044] The second dielectric layer 308 is then patterned to define interconnects 310, as illustrated in FIG. 4d, preferably using conventional lithography processes as described above. The interconnects 310 formed in the second dielectric layer 308 are positioned over the contact/via openings 306 in the organosilicate layer 304. Thereafter, both the interconnects 310 and contacts/vias 306 are etched to expose the surface of the conductive features 301, using reactive ion etching or other anisotropic etching techniques.

[0045] Referring to FIG. 4e, the interconnects 310 and contacts/vias 306 are filled with a conductive material 314 such as aluminum, copper, tungsten, or combinations thereof. Typically, copper is used to fill the interconnects 310 and contacts/vias 306 due to its low resistivity (resistivity about 1.7 μ-cm). The conductive material 314 is deposited using chemical vapor deposition, physical vapor deposition, electroplating, or combinations thereof, to form the damascene structure. Preferably, a barrier layer 312 such as tantalum, tantalum nitride, or other suitable barrier material is first deposited conformably on the sidewalls of the interconnects 310 and contacts/vias 306 to prevent metal migration into the surrounding dielectric layers 302, 308 as well as the organosilicate layer 304.

Claims

1. A method of thin film deposition, comprising:

- positioning a substrate in a deposition chamber;
- providing a gas mixture to the deposition chamber, wherein the gas mixture comprises an - organosilane compound and an oxygen-containing gas; and
- applying an electric field to the gas mixture in the deposition chamber to form an organosilicate layer on the substrate.

2. A method forming an organosilicate layer on a substrate, comprising:

positioning a substrate in a deposition chamber;
providing a gas mixture to the deposition chamber, wherein the gas mixture comprises an organosilane compound and an oxygen-containing gas; and
applying an electric field to the gas mixture in the deposition chamber to form an organosilicate layer on the substrate.

3. A method of forming a device, comprising:

providing a substrate having conductive features formed thereon; and
forming an organosilicate layer over the conductive features, wherein the organosilicate layer is formed by applying an electric field to a gas mixture comprising an organosilane compound and an oxygen-containing gas.

4. The method of claim 3 wherein the conductive features are formed of one or more materials selected from the group consisting of copper, aluminum, tungsten, and combinations thereof.

5. A method of fabricating a damascene structure, comprising

forming a first dielectric layer on a substrate;
forming an organosilicate layer on the first dielectric layer, wherein the organosilicate layer is formed by applying an electric field to a gas mixture comprising an organosilane compound and an oxygen-containing gas;
patterning the organosilicate layer to define contacts/vias therethrough;
forming a second dielectric layer on the patterned organosilicate layer;
patterning the second dielectric layer to define interconnects therethrough, wherein the interconnects are positioned over the contacts/vias defined in the organosilicate layer;
etching the first dielectric layer to form contacts/vias therethrough; and
filling the contacts/vias and the interconnects with a conductive material.

6. The method of claim 5 wherein the first dielectric layer and the second dielectric layer are each selected from the group consisting of amorphous carbon, fluorinated amorphous carbon, parylene, fluorinated silicate glass (FSG). AF_4, BCB, silicon carbide, oxynitride, and combinations thereof.

7. The method of claim 5 wherein the conductive material filling the contacts/vias and interconnects is selected from the group consisting of copper, aluminum, tungsten, and combinations thereof.

8. The method of any of the preceding claims wherein the organosilane compound has a general formula $Si_aC_bH_cO_d$ where a has a range between 1 and 2, b has a range between 1 and 10, c has a range between 6 and 30, and d has a range between 0 and 6.

9. The method of claim 8 wherein the organosilane compound is selected from the group of methylsilane ($SiCH_6$), dimethylsilane (SiC_2H_8), trimethylsilane (SiC_3H_{10}), tetramethylsilane (SiC_4H_{12}), methoxysilane ($SiCH_6O$), dimethyldimethoxysilane ($SiC_4H_{12}O_2$), diethyldiethoxysilane ($SiC_8H_{18}O_2$), dimethyldiethoxysilane ($SiC_6H_{16}O_2$), diethyldimethoxysilane ($SiC_6H_{16}O_2$), hexamethyldisiloxane ($Si_2C_6H_{18}O$), bis(methylsilano)methane ($Si_2C_3H_{12}$), 1,2-bis(methylsilano)ethane ($Si_2C_4H_{14}$), and combinations thereof.

10. The method of any of the preceding claims wherein the oxygen-containing gas is selected from the group of nitrous oxide (N_2O), oxygen (O_2), ozone (O_3), carbon monoxide (CO), carbon dioxide (CO_2), and combinations thereof.

11. The method of claim any of the preceding claims wherein the electric field applied to the gas mixture in the deposition chamber is a radio frequency (RF) power.

12. The method of claim 11 wherein the RF power is within the range of 1 watts/cm^2 to 500 watts/cm^2.

13. The method of any of the preceding claims wherein the deposition chamber is maintained at a pressure between 1 torr to 500 torr.

14. The method of any of the preceding claims wherein the organosilane compound is provided to the deposition chamber at a flow rate in a range of 50 sccm to 1000 seem.

15. The method of any of the preceding claims wherein the oxygen-containing gas is provided to the deposition chamber at a flow rate in a range of 10 seem

to 1000 seem.

16. The method of any of the preceding claims wherein the ratio of the oxygen-containing gas to the organosilane compound is 1:1 to 1:5.

17. The method of any of the preceding claims wherein the deposition chamber is maintained at a temperature between 50 °C to 500 °C.

18. The method of any of the preceding claims wherein the organosilicate layer is formed on the substrate at a rate greater than 0.1 microns per minute.

19. The method of any of the preceding claims further comprising the step of annealing the organosilicate layer formed on the substrate.

20. The method of claim 19 wherein the annealing step is performed at a temperature between 200 C to 500 C.

21. The method of claim 19 wherein the annealing step is performed in an atmosphere comprising one or more gases selected from the group of nitrogen (N_2), hydrogen (H_2), and oxygen (O_2).

22. The method of claim 19 wherein the annealing step is performed for a time less than 30 minutes.

23. A computer storage medium containing a software routine that, when executed, causes a general purpose computer to control a deposition chamber according to the method of any of the preceding claims.

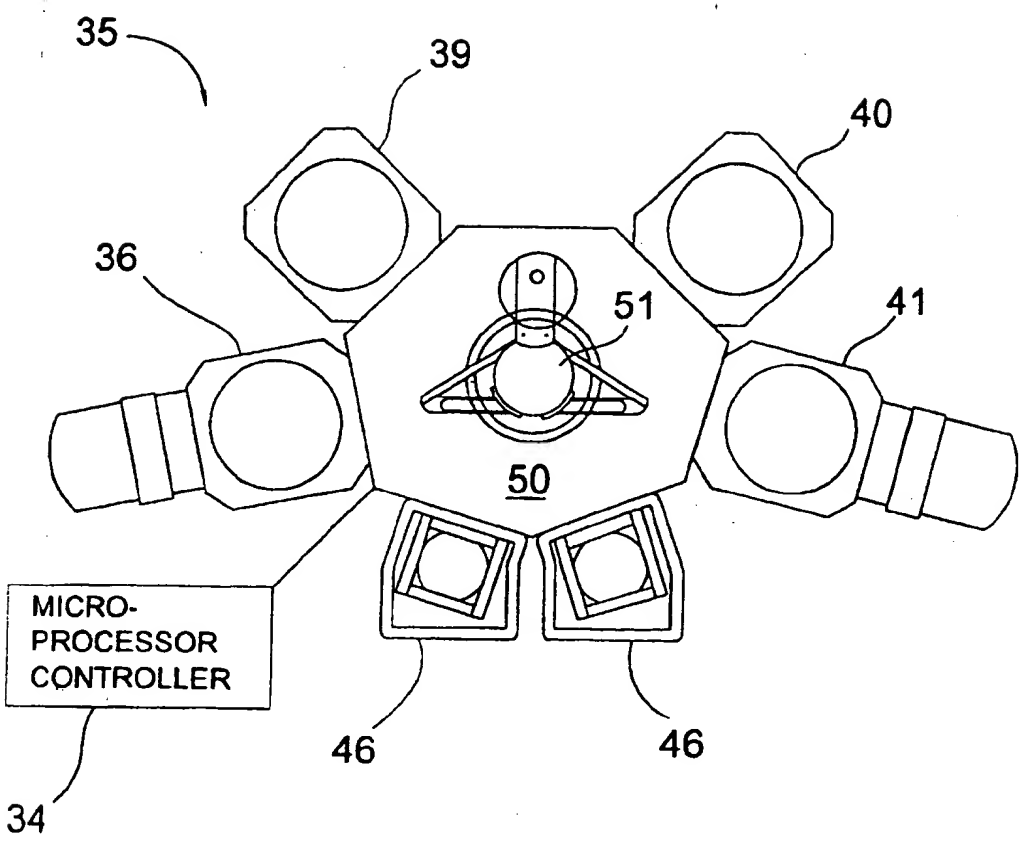

FIG. 1

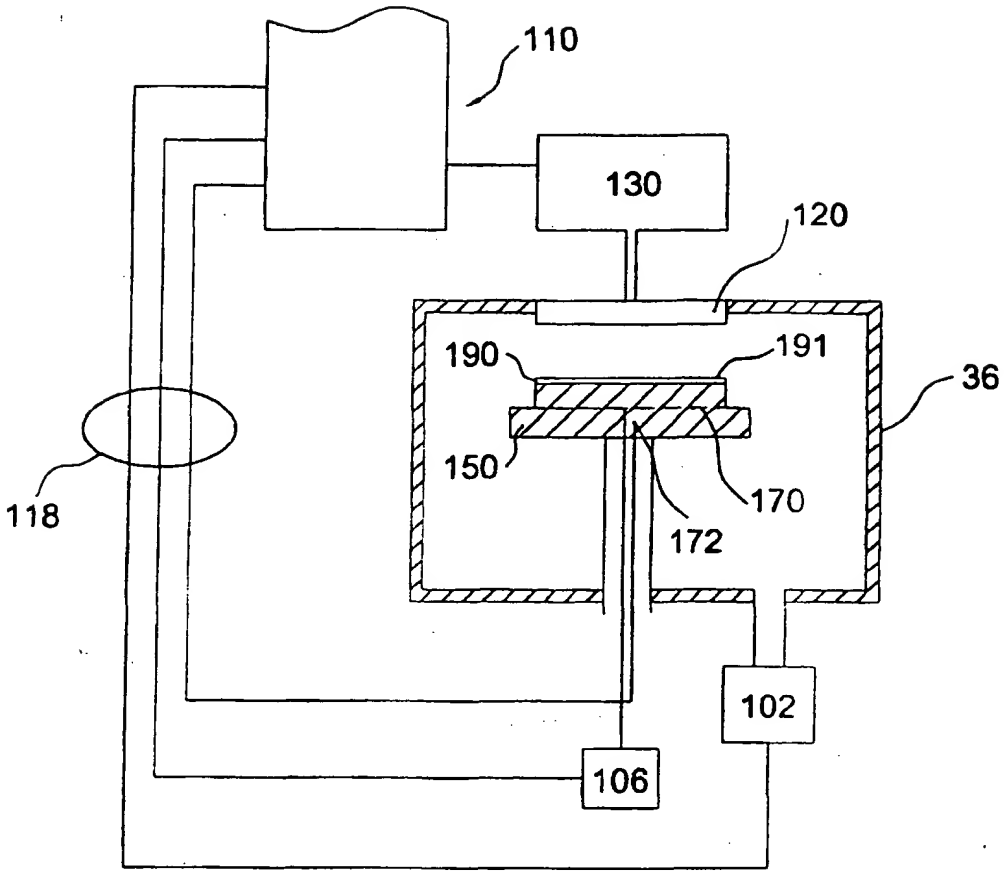

Fig.2

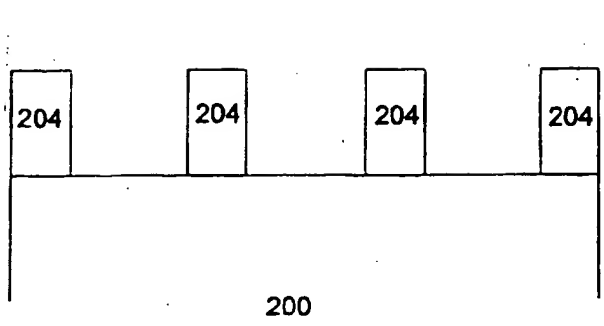

Fig.3a

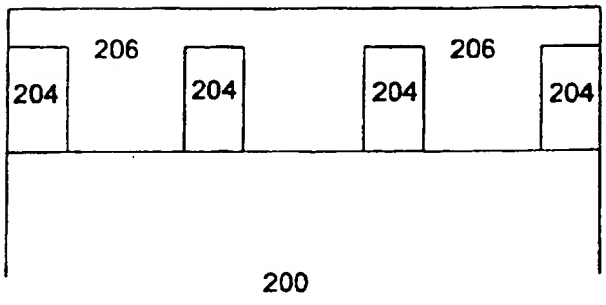

Fig.3b

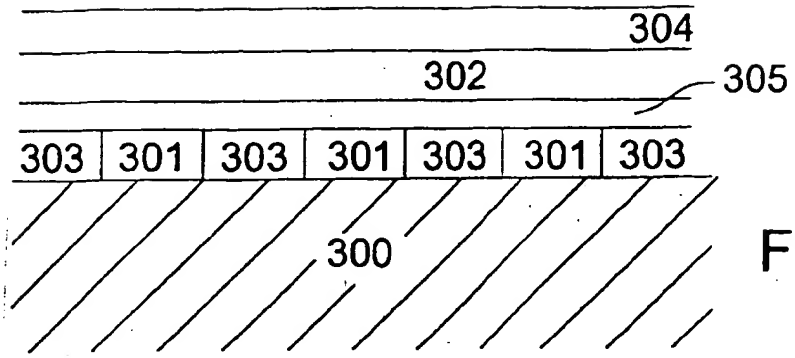

Fig. 4a

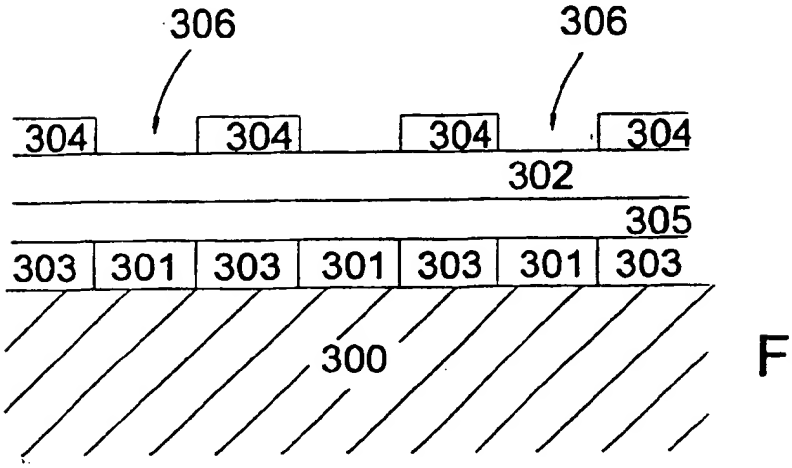

Fig. 4b

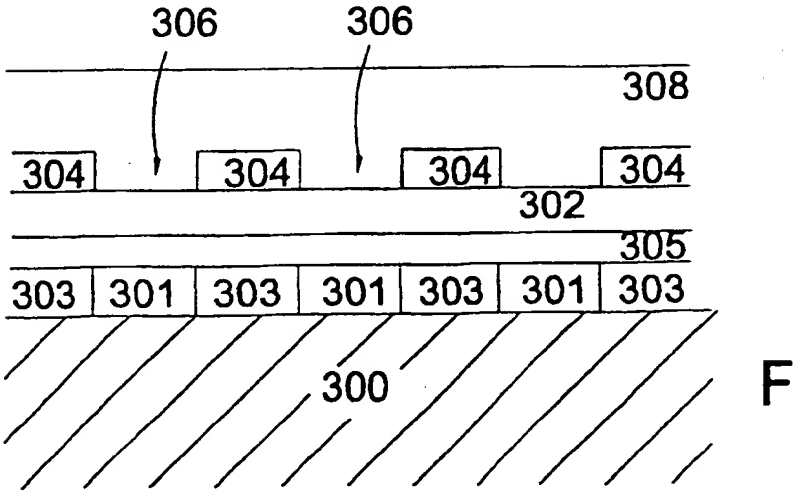

Fig. 4c

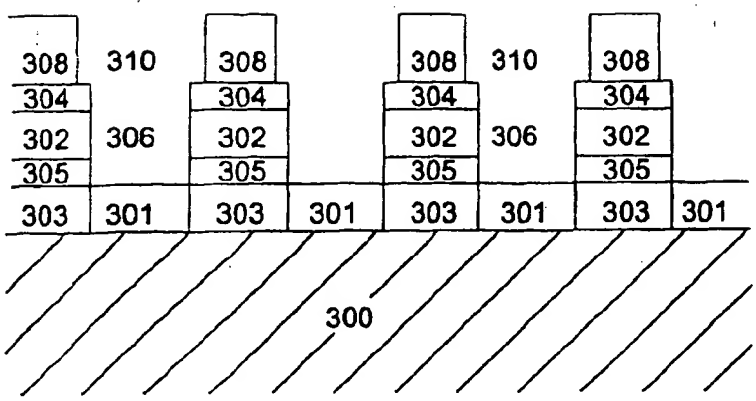
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Fig. 4d

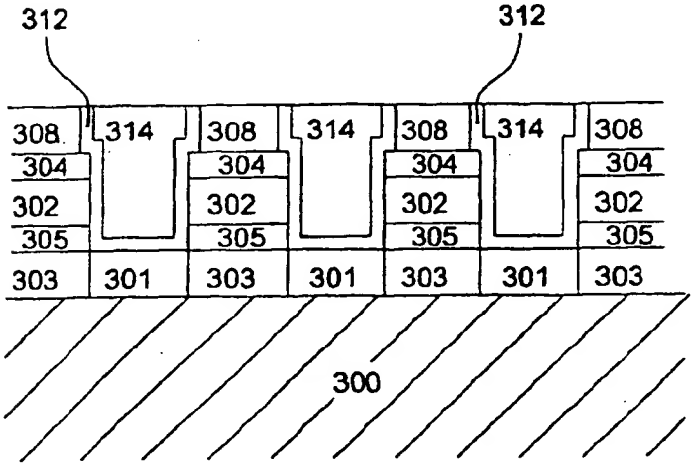
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Fig. 4e

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EUROPEAN SEARCH REPORT

Application Number
EP 01 12 3151

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Place of search	Date of completion of the search	Examiner
THE HAGUE	15 February 2002	Ekhult, H

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